



Progressive Education Society's  
**MODERN COLLEGE OF ARTS SCIENCE & COMMERCE**

Shivajinagar, Pune- 411 005.

- NAAC re-accredited with 'A' Grade ■ Best College Award, University of Pune
- College with Potential for Excellence, by UGC

**DEPARTMENT OF ELECTRONIC SCIENCE**

Organizes

**STATE LEVEL WORKSHOP ON**

**"DIGITAL SYSTEM DESIGN USING VHDL ON CPLD BOARD"**  
10<sup>th</sup> and 11<sup>th</sup> February 2012

■ **Who can Participate ?**

P. G. Students, Research Students and Faculty of Electronic Science/ Electronic & Telecommunication/ Instrumentation/ Physics.

■ **Prerequisites :**

- Experience of digital circuit design
- Knowledge of High Level Programming Language

■ **Registration procedure :**

- Participant can confirm their participation by sending e-mail to : [modern\\_msc@yahoo.co.in](mailto:modern_msc@yahoo.co.in)
- Organizer will send soft copy of an application form and batch number to participant by e-mail
- Participant will submit softcopy of application form and DD number through e-mail
- Send DD of registration fee payable to "**Principal, Modern College, Pune- 5**" along with hardcopy of registration form to Prof. D.B. Gaikwad, Organizing Secretary, State level workshop on Digital System Design using VHDL on CPLD board, Department of Electronic Science, Modern College of Arts, Science & Commerce, Shivajinagar, Pune- 411 005.

**Last Date : 24<sup>th</sup> January 2012**

**Number of participants limited to 30**

The first 30 participants sending registration forms and DD will be registered as participant of the workshop.

***RUSH YOUR ENTRIES***

■ **Registration Fee :**

Student Participant : Rs. 600/-  
Faculty Member : Rs. 800/-

The registration fee covers local hospitality, study material and laboratory session.

■ **Accommodation :**

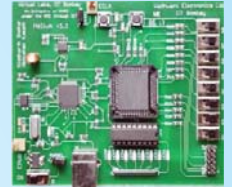
The College does not have guest house to accommodate the participants. However, organizers will help in making accommodation available at nearby places if required. The accommodation charges will be borne by respective participant. If accommodation is needed it may be communicate on before 25<sup>th</sup> January 2012.

■ **T.A. and D.A. :**

T.A. and D.A. expenses should be borne by the respective college/ institute.

■ **Background :**

- FPGA/ CPLDs are getting predominant in semiconductor world day- by- day, due to their increased densities & frequencies, reduced cost, and reduced power consumption, non volatile feature (CPLD).
- FPGA/ CPLDs are finding extensive applications in Video Processing, Networking, Medical Imaging, Consumer Electronics, Defense, Aerospace, Satellites, Cell Phones, and many more. Further growing technological requirements have created and unprecedented demand for FPGAs/ CPLD in VLSI and Embedded technologies space. Which fuelled huge demand for the FPGA professionals.
- This workshop is an initiative to create such FPGA/ CPLD Professionals to fill this huge demand.



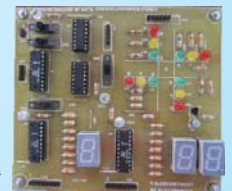
■ **Programme Contents :**

**(Includes Lecture, Demonstration from Experts and Hands on Training)**

- **Introduction to CPLD architecture**
- **Introduction to VHDL programming**
- **Digital System Design on CPLD board using VHDL**
- **CPLD interfacing techniques : Displays, Stepper motor, Traffic light controller etc.**
- **System integration**

■ **Uniqueness of Workshop :**

- Hands-On training
- 30% Theory, 70% Practical Sessions
- **State- of- art CAD Tools :** Quartus- II, University Altera programme simulator
- **Hardware Tools :** Altera CPLD Kit, State of Art Pcs, Interfacing board



■ **Contacts :**

Chairman : Prof. S. R. Chaudhari 9822682812  
Organizing Secretary : Prof. D. B. Gaikwad 9881509515  
Co-ordinator : Mr. G. M. Tarate 7709945354